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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,466	NISHITOBA, SHIGEO	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-26* is/are allowed.

6)☒ Claim(s) *1-6 and 9-13* is/are rejected.

7)☒ Claim(s) *7,8,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *07 January 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/22/03 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6, 9, 10, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Emeigh et al. (USP 5,767,698).

With respect to claim 1, each of Figures 4 and 5 of the Emeigh et al. reference discloses a driving circuit, which includes: a first current mirror circuit (32 in Figure 4, or 32' in Figure 5) which outputs a plurality of output currents (at the drains terminal of transistors T1-T3 in Figure 5, or at the drains terminals of transistors T1'-T3'), each of which corresponds to a reference current (reference current IREF from circuit 20); a reference input terminal (drain of transistor T0 in Figure 4, drain of T0' in Figure 5) for supplying the reference current (IREF from circuit

20) to the first current mirror circuit (32 in Figure 4, 32' in Figure 5); and a second current mirror circuit (34 in Figure 4, or 34' in Figure 5) which converts a polarity of an output current (the current at the drain terminal of transistor T3 in Figure 4, or at the drain terminal of transistor T3' in Figure 5) from a final stage (T3 in Figure 4, or T3' in Figure 5) of said first current mirror circuit (32 in Figure 4, or 32' in Figure 5) and outputs the converted output current (at the drain terminal of transistor T7 in Figure 4, or at the drain terminal of transistor T7' in Figure 5.

With respect to claim 2, the Emeigh et al. reference shows that the first current mirror circuit (32 in Figure 4, 32' in Figure 5) includes: a power supply terminal (Vdd in Figure 4, GND in Figure 5) to which power is supplied (Vdd in Figure 4, GND in Figure 5); a first circuit (T0 in Figure 4, T0' in Figure 5) provided between said reference current input terminal and said power supply terminal, to determine said plurality of output currents (drains of transistors T1-T3 in Figure 4, or drains T1'-T3' in Figure 5); a common power supply line which extends from said power supply terminal (inherently because all power supplies Vdd in the circuit are tied together, or all the grounds GND in the circuit are tied together); a plurality of output terminals (drains of transistors T1 and T2 in Figure 4, or drains of transistors T1' and T2' in Figure 5); a plurality of second circuits (T1-T2 in Figure 4, T1'-T2' in Figure 5) provided between said common power supply line (Vdd in Figure 4, GND in Figure 5) and said plurality of output terminals, to output a part of said plurality of output currents (drains of T1 and T2 in Figure 4, drains of T1' and T2' in Figure 5) determined by said first circuit (T0 in Figure 4, T0' in Figure 5) through said plurality of output terminals (drains of T1 and T2 in Figure 4, drains of T1' and T2' in Figure 5); and a third circuit (T3 in Figure 4, T3' in Figure 5) provided at a next stage of said plurality of second circuits (T1-T2 in Figure 4, T1'-T2' in Figure 5) as said final stage (T3 in Figure 4, T3' in Figure

5) of said first current mirror circuit, to output said output current (at the drain terminal of transistor T3 in Figure 4, or at the drain terminal of transistor T3' in Figure 5) determined by said first circuit (T0 in Figure 4, T0' in Figure 5).

With respect to claim 3, the second current mirror circuit (34 in Figure 4, 34' in Figure 5) converts the polarity of the output current (drain of T3 in Figure 4, or drain of T3' in Figure 5) outputted from the third circuit (T3 in Figure 4, T3' in Figure 5) and outputs said converted output current (at the drain of T7 in Figure 4, or at the drain of T7' in Figure 5) through a reference current output terminal (drain of T7 in Figure 4, or drain of T7' in Figure 5).

With respect to claim 6, Figure 5 of the Emeigh et al. reference discloses that the first circuit (T0'), the second circuits (T1'-T2') and the third circuit (T3') included in said first current mirror circuit (32') are constituted by P-channel MOS transistors, and said second current mirror circuit (34') is constituted by N-channel MOS transistors.

With respect to claim 9, Figure 4 of the Emeigh et al. shows that the first current mirror circuit (32) includes: a ground terminal (GND) to which is connected to a ground; a first circuit (T0) provided between said reference current input terminal and said ground terminal, to determine said plurality of output currents (drains of transistors T1-T3); a common ground line which extends from the ground terminal (inherently because all the grounds GND in the circuit are tied together); a plurality of output terminals (drains of transistors T1 and T2); a plurality of second circuits (T1-T2 in Figure 4) provided between said common ground line and said plurality of output terminals, to output a part of said plurality of output currents (drains of T1 and T2) determined by said first circuit (T0) through said plurality of output terminals (drains of T1 and T2); and a third circuit (T3) provided at a next stage of said plurality of second circuits (T1-

T2) as said final stage (T3) of said first current mirror circuit (32), to output said output current (at the drain terminal of transistor T3) determined by said first circuit (T0).

With respect to claim 10, Figure 4 of the Emeigh et al. reference shows that the second current mirror circuit (34) converts the polarity of the output current (drain of T3) outputted from the third circuit (T3) and outputs said converted output current (at the drain of T7) through a reference current output terminal (drain of T7).

With respect to claim 13, Figure 4 of the Emeigh et al. reference shows that the first circuit (T0), said second circuits (T1, T2) and the third circuit (T3) included in said first current mirror circuit (32) are constituted by N-channel MOS transistors, and said second current mirror circuit (34) is constituted by P-channel MOS transistors.

4. Claims 1-4, 6, 9-11 and 13 are also rejected under 35 U.S.C. 102(e) as being anticipated by Geysen (USP 6,229,376).

With respect to claim 1, the Geysen reference discloses a circuit (either Figure 2 or Figure 6, lines 3-19 of Col. 3, lines 49-51 of Col. 7, and also lines 35-39 of Col. 8) which includes: a first current mirror circuit (110, 120, 130 and 140 in Figure 2; or 110', 120', 130' and 140' in Figure 6) which outputs a plurality of output currents (at the collectors of transistors 120 or 120', 130 and 140 in Figure 2; or at the drains of transistors 120', 130' and 140' in Figure 6), each of which corresponds to a reference current (current input 100, and see lines 49-51 of Col. 7); and a second current mirror circuit (170 and 180 in Figure 2, or 170' and 180' in Figure 6) which converts a polarity of an output current (the current at collector of transistor 140 in Figure 2, or at the drain of transistor 140' in Figure 6) outputted from a final stage (140 in Figure 2, or 140' in Figure 6) of said first current mirror circuit and outputs the converted output current (at

the collector of transistor 180 in Figure 2, or at the drain of transistor 180' in Figure 6), see Col. 11, lines 43-63.

With respect to claim 2, Figure 2 of the Geysen reference shows that the first current mirror circuit (110, 120, 130 and 140 in Figure 2; or 110', 120', 130' and 140' in Figure 6) includes: a reference current input terminal (100) to which said reference current is supplied (lines 49-51 of Col. 7, and lines 46-48 of Col. 11); a power supply terminal (Vcc) to which power is supplied (Vcc); a first circuit (110 in Figure 2, or 110' in Figure 6) provided between said reference current input terminal (100) and said power supply terminal (Vcc), to determine said plurality of output currents; a common power supply line (the line connecting the emitters of transistors 110, 120, 130 and 140 together in Figure 2; or the line connecting the drains of transistors 110', 120', 130' and 140' together in Figure 6) which extends from said power supply terminal (Vcc); a plurality of output terminals (150 and 160); a plurality of second circuits (120 and 130 in Figure 2, or 120' and 130' in Figure 6) provided between said common power supply line and said plurality of output terminals, to output a part of said plurality of output currents determined by said first circuit through said plurality of output terminals (150 and 160 in Figure 2, or 150' and 160' in Figure 6); and a third circuit (140 in Figure 2 or 140' in Figure 6) provided at a next stage of said plurality of second circuits (120 and 130 in Figure 2, or 120' and 130' in Figure 6) as said final stage (140 in Figure 2, or 140' in Figure 6) of said first current mirror circuit, to output said output current (at the collector of transistor 140 in Figure 2, or at the drain of transistor 140' in Figure 6) determined by said first circuit.

With respect to claim 3, the second current mirror circuit converts the polarity of the output current (at the collector of transistor 140 in Figure 2, or at the drain of transistor 140' in

Figure 6) outputted from the third circuit (140 in Figure 2 or 140' in Figure 6) and outputs said converted output current (at the collector of transistor 180 in Figure 2, or at the drain of transistors 180' in Figure 6) through a reference current output terminal (230).

With respect to claim 4, Figure 2 of the Geysen reference shows that the first circuit (110), said second circuits (120, 130) and said third circuit (140) included in said first current mirror circuit (110, 120, 130 and 140) are constituted by PNP transistors, and the second current mirror circuit (170, 180) is constituted by NPN transistors.

With respect to claim 6, Figure 6 of the Geysen reference discloses that the first circuit (110'), said second circuits (120', 130') and the third circuit (140') included in said first current mirror circuit (110', 120', 130' and 140') are constituted by P-channel MOS transistors, and said second current mirror circuit (170', 180') is constituted by N-channel MOS transistors.

With respect to claim 9, as discussed on lines 35-39 of Col. 8 of the Geysen reference, the PNP and NPN transistors in Figure 2 can be changed to NPN and PNP transistors (reversed Figure 2), respectively (i.e., PNP transistors 110, 120, 130 and 140 in Figure 2 are changed to NPN transistors, and NPN transistors 170, 180, 190 and 200 in Figure 2 are changed to PNP transistors); the ground terminal in Figure 2 is changed to the power supply Vcc terminal; and the power supply Vcc terminal in Figure 2 is changed to the ground terminal. Similarly, the P-channel and N-channel transistors in Figure 6 are changed to the N-channel and P-channel transistors (reversed Figure 6), respectively; the ground terminal in Figure 6 is changed to the power supply Vcc terminal; and the power supply Vcc terminal in Figure 6 is changed to the ground terminal. Thus, claim 9 is rejected for the similar reasons as claim 2, e.g., the first current mirror circuit (110, 120, 130 and 140 in the reversed Figure 2, see lines 35-39 of Col. 8;

or 110', 120', 130' and 140' in the reversed of Figure 6, see lines 35-39 of Col. 8) including: a reference current input terminal (100) to which said reference current is supplied (lines 49-51 of Col. 7, and lines 46-48 of Col. 11); a ground terminal (ground) which is connected to a ground; a first circuit (110 in the reversed Figure 2, or 110' in the reversed Figure 6) provided between the reference current input terminal (100) and the ground terminal (ground), to determine said plurality of output currents; a common ground line (the line connecting the emitters of transistors 110, 120, 130 and 140 together in the reversed Figure 2; or the line connecting the source of transistors 110', 120', 130' and 140' together in the reversed Figure 6) which extends from the ground terminal (ground); a plurality of output terminals (150 and 160); a plurality of second circuits (120 and 130 in the reversed Figure 2, or 120' and 130' in the reversed Figure 6) provided between the common ground line and the plurality of output terminals, to output a part of said plurality of output currents determined by the first circuit through the plurality of output terminals (150 and 160 in the reversed Figure 2, or 150' and 160' in the reversed Figure 6); and a third circuit (140 in the reversed Figure 2 or 140' in the reversed Figure 6) provided at a next stage of the plurality of second circuits (120 and 130 in the reversed Figure 2, or 120' and 130' in the reversed Figure 6) as the final stage (140 in the reversed Figure 2, or 140' in the reversed Figure 6) of the first current mirror circuit, to output the output current (at the collector of transistor 140 in the reversed Figure 2, or at the drain of transistor 140' in the reversed Figure 6) determined by said first circuit.

With respect to claim 10, the second current mirror circuit converts the polarity of the output current (at the collector of transistor 140 in the reversed Figure 2, or at the drain of transistor 140' in the reversed Figure 6) outputted from the third circuit (140 in the reversed

Figure 2 or 140' in the reversed Figure 6) and outputs the converted output current (at the collector of transistor 180 in the reversed Figure 2, or at the drain of transistors 180' in the reversed of Figure 6) through a reference current output terminal (230).

With respect to claim 11, the reversed Figure 2 (lines 35-39 of Col. 8) as discussed above with regard to claim 9, meets the limitation in claim 11 that the first circuit (110), said second circuits (120, 130) and said third circuit (140) included in the first current mirror circuit (110, 120, 130 and 140) are constituted by NPN transistors, and the second current mirror circuit (170, 180) is constituted by PNP transistors.

With respect to claim 13, the reversed Figure 6 (lines 35-39 of Col. 8) as discussed above with regard to claim 9, meets the limitation in claim 13 that the first circuit (110'), said second circuits (120', 130') and the third circuit (140') included in said first current mirror circuit (110', 120', 130' and 140') are constituted by N-channel MOS transistors, and said second current mirror circuit (170', 180') is constituted by P-channel MOS transistors.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emeigh et al. (USP 5,767,698) in view of Nayebi et al. (USP 6,384,638).

With respect to claim 4, Figure 5 of the Emeigh et al. reference discloses a driving circuit as discussed above with regard to the 102(b) rejection which includes all the limitations of this

claim except the circuit is fabricated using bipolar technology. However, the Nayebi et al. reference teaches that using bipolar technology to fabricate a circuit is less expensive than using BiCMOS technology (see Col. 4, lines 5-6 of the Nayebi et al. reference). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the Emeigh et al. reference to fabricate the driving circuit in Figure 5 of the Emeigh et al. reference using bipolar technology as taught by the Nayebi et al. reference instead of BiCMOS technology, e.g., each of the N-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by an NPN transistor and each of the P-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by a PNP transistor, for the purpose saving cost. Thus, this modification meets all the limitations of claim 4 because the first circuit (T0'), the second circuits (T1' and T2') and the third circuit (T3') included in the first current mirror circuit (32') are constituted by PNP transistors (because each of the P-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by a PNP transistor as discussed in the modification), and the second mirror circuit (34') is constituted by NPN transistors (because each of the N-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by an NPN transistor as discussed in the modification).

With respect to claim 11, Figure 4 of the Emeigh et al. reference discloses a driving circuit as discussed above with regard to the 102(b) rejection which includes all the limitations of this claim except the circuit is fabricated using bipolar technology. However, the Nayebi et al. reference teaches that using bipolar technology to fabricate a circuit is less expensive than using BiCMOS technology (see Col. 4, lines 5-6 of the Nayebi et al. reference). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to

modify the Emeigh et al. reference to fabricate the driving circuit in Figure 4 of the Emeigh et al. reference using bipolar technology as taught by the Nayebi et al. reference instead of BiCMOS technology, e.g., each of the N-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by an NPN transistor and each of the P-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by a PNP transistor, for the purpose saving cost. Thus, this modification meets all the limitations of claim 11 because the first circuit (T0), the second circuits (T1 and T2) and the third circuit (T3) included in the first current mirror circuit (32) are constituted by NPN transistors (because each of the N-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by an NPN transistor as discussed in the modification), and the second mirror circuit (34) is constituted by PNP transistors (because each of the P-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by a PNP transistor as discussed in the modification).

7. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emeigh et al. (USP 5,767,698) in view of Nayebi et al. (USP 6,384,638), and further in view of Kipnis (USP 6,326,836).

With respect to claim 5, the driving circuit as discussed in the above modification (Figure 5 of Emeigh et al. in view of Nayebi et al.) with regard to the rejection of claim 4 meets all the limitations of this claim except for the limitation that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensation circuit. However, the Kipnis reference discloses that each of the current mirror circuits in Figure 2 includes a current compensation circuit (i.e., current mirror circuit 203, 205 and 207 including a current compensation circuit 205; current mirror circuit 209, 211 and 213 including a current compensation circuit 211; and current mirror circuit 215, 217 and 219 including a current

compensation circuit 217) for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit (Col. 1, lines 36-62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the first and second current mirror circuits (32' and 34') in the above modification (Figure 5 of Emeigh et al. in view of Nayebi et al.) with a base current compensation circuit as taught by the Kipnis reference for the purpose of preventing excessive loading of the base connections of the transistors in each of the current mirror circuits. Thus, this modification meets all the limitations of claim 5.

With respect to claim 12, the driving circuit as discussed in the above modification (Figure 4 of Emeigh et al. in view of Nayebi et al.) with regard to the rejection of claim 11 meets all the limitations of this claim except for the limitation that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensation circuit. However, the Kipnis reference discloses that each of the current mirror circuits in Figure 2 includes a current compensation circuit (i.e., current mirror circuit 203, 205 and 207 including a current compensation circuit 205; current mirror circuit 209, 211 and 213 including a current compensation circuit 211; and current mirror circuit 215, 217 and 219 including a current compensation circuit 217) for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit (Col. 1, lines 36-62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the first and second current mirror circuits (32 and 34) in the above modification (Figure 4 of Emeigh et al. in view of Nayebi et al.) with a base current compensation circuit as taught by the Kipnis reference for the purpose of preventing excessive

loading of the base connections of the transistors in each of the current mirror circuits. Thus, this modification meets all the limitations of claim 12.

8. Claims 5 and 12 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Geysen (USP 6,229,376) in view of Kipnis (USP 6,326,836).

With respect to claim 5, Figure 2 of the Geysen reference, as discussed above with regard to claims 1-4, discloses all the limitations of this claim except for the limitation that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensation circuit. However, the Kipnis reference discloses that each of the current mirror circuits in Figure 2 includes a current compensation circuit (i.e., current mirror circuit 203, 205 and 207 including a current compensation circuit 205; current mirror circuit 209, 211 and 213 including a current compensation circuit 211; and current mirror circuit 215, 217 and 219 including a current compensation circuit 217) for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit (Col. 1, lines 36-62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the first and second current mirror circuits in Figure 2 of the Geysen reference with a base current compensation circuit for the purpose of preventing excessive loading of the base connections of the transistors in each of the current mirror circuits.

With respect 12, the reversed Figure 2 of the Geysen reference, as discussed above with regard to claims 9-11, discloses all the limitations of this claim except for the limitation that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensation circuit. However, the Kipnis reference discloses that each of the current mirror circuits in Figure 2 includes a current compensation circuit (i.e., current mirror circuit 203, 205

and 207 including a current compensation circuit 205; current mirror circuit 209, 211 and 213 including a current compensation circuit 211; and current mirror circuit 215, 217 and 219 including a current compensation circuit 217) for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit (Col. 1, lines 36-62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the first and second current mirror circuits in the reversed Figure 2 of the Geysen reference with a base current compensation circuit, again for the purpose of preventing excessive loading of the base connections of the transistors in each of the current mirror circuits.

Allowable Subject Matter

9. Claims 16-26 are allowed.

Claim 16 is allowed because the prior art of record does not disclose or suggest a constant driving apparatus comprising a plurality of driving circuits connected through terminals in series, wherein each of the driving circuits includes a first current mirror circuit which outputs a plurality of plurality of output currents, each of which corresponds to a reference current, and a second current mirror circuit which converts a polarity of an output current outputted from a final stage of the first current mirror circuit and outputs the converted output current.

Claims 17-26 are allowed because they depend on claim 16.

10. Claims 7, 8, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the power supply terminal is pulled out from a center of the common power supply line.

Claim 8 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the power supply terminal is pulled out from a plurality of positions of the common power supply line.

Claim 14 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the ground terminal is pulled out from a center of the common ground line.

Claim 15 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the ground terminal is pulled out from a plurality of positions of the common ground supply line.

Response to Arguments

11. Applicant's arguments filed on 5/22/03 have been fully considered but they are not persuasive.

With respect to the 102(b) rejection under Emeigh et al. (USP 5,767,698), applicant argues: "indeed, 'correspond' is defined in Webster's Dictionary as 'to be in agreement or conformity, match, to be similar or analogous'. The outputs of transistors T1-T3 in Emeigh are

scaled up at three to five times the current of the reference current IREF and therefore do not 'correspond' to the reference current". However, this argument is not persuasive because the claim does not clearly recited that each of the output currents equals to the reference current. Furthermore, according to the dictionary, "correspond" is very broad and is not necessary to be 'the same'. Note that "correspond" is defined as 'analogous', and outputs of transistors T1-T3 in Emeigh are scaled up at three to five times the current of the reference current IREF and therefore meets the definition of "correspond" as 'analogous'.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Note that the Nayebi et al. reference (USP 6,384,638) teaches that using bipolar technology to fabricate a circuit is less expensive than using BiCMOS technology (see Col. 4, lines 5-6 of the Nayebi et al. reference). Therefore, the 103(a) rejection (Emeigh et al. in view of Nayebi et al.) is proper since using bipolar technology is less expensive than using BiCMOS technology. Note that the "correspond" is defined as 'analogous' and therefore meets the claim limitation as discussed above in the response to arguments under 102(b) rejection.

Also note that the Kipnis reference teaches that each of the current mirror circuits in Figure 2 includes a current compensation circuit (i.e., current mirror circuit 203, 205 and 207

including a current compensation circuit 205; current mirror circuit 209, 211 and 213 including a current compensation circuit 211; and current mirror circuit 215, 217 and 219 including a current compensation circuit 217) for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit (Col. 1, lines 36-62). Therefore, the 103(a) rejection (Emeigh et al. in view of Nayebi et al., and further in view of Kipnis) is proper since providing the current compensation circuit to the current mirror would have an advantage such as preventing excessive loading of the base connections of the transistors in the current mirror circuit. Note that the "correspond" is defined as 'analogous' and therefore meets the claim limitation as discussed above in the response to arguments under 102(b) rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

LN
Date: 8/19/03

Long Nguyen
Art Unit: 2816